Scheduling Based Dynamic Power Management Technique for offline Optimization of Energy in Multi Core Processors

Hamayun Khan
Department of Electrical Engineering
Gomal University
D.I.Khan, KPK, Pakistan
hamayunkhan815@ymail.com

Sheeraz Ahmad
Department of Computer Science
Iqra National Unviersity
Peshwar,KPK,, Pakistan
sheeraz.ahmad@inu.edu.pk

Nasir Saleem
Department of Electrical Engineering
Gomal University
D.I.Khan, KPK, Pakistan
nasirsaleem@gu.edu.pk

M.Usman Hashmi
Department of Computer Science
Superior University, Lahore Campus
Lahore, Punjab, Pakistan
usmanhashmi06@hotmail.com

Qaisar Bashir
Department of Electrical Engineering
University of Lahore
Lahore, Punjab, Pakistan
qaisarbashir19@yahoo.com

***Abstract* - The criteria to judge the capacity of computational systems is changing with the advancement in technology. Earlier, they were judged only on the basis of computational capacity but now a day, power and energy optimization is one of the key parameters for their selection. The purpose of energy optimization is to prolong the battery life of all the battery operated devices especially in embedded systems. An Offline Scheduling Algorithm technique is proposed that migrate task load to the core that has less thermal values in response to a threshold temperature this technique also considers other thermal problems which affects the power, reliability and performance of multi-core system. Hardware technique on their own is insufficient so it must be combined with other software techniques to decide when and where optimization policies are applied to minimum energy consumption. This paper focuses on most popular optimization techniques Dynamic Voltage and Frequency Scaling (DVFS), Dynamic Power Management (DPM) and Dynamic Thermal Management (DTM) and their extensions. The paper also includes the thermal issues which are raised due to high temperature in multi-core platforms. It also highlights that how energy efficient techniques can be used beyond simple energy saving The simulation results shows that the proposed technique reduces almost 4.3℃ temperatures at 17% utilization and the energy utilization is 240.43 J which is 5.21 % improved as compare to the global EDF Scheduling technique used previously.**

Index Terms – Dynamic Voltage and Frequency Scaling, Dynamic Power Management, Dynamic Thermal Management, Optimization.

I. INTRODUCTION

We are living in the world which is evolving at much faster rate than ever before. Today embedded systems are everywhere from simple toaster to a large scale telecommunication system, defence system and many others. The growth rate in embedded systems is almost 10% per year and it is predicted that till 2020 almost 40 billion embedded devices worldwide. We generally define embedded system as a sub component of a larger system. Combination of hardware and software, designed to perform dedicated functionality. While designing embedded systems, there come few challenges such as size, cost, power consumption and reliability. Most of the embedded systems are battery operated. To achieve the maximum performance while using minimum power consumption is the major design challenge in all electronic/embedded systems. According to Moore's law number of transistors on a chip is doubling in almost every 18 months [1]. The continuous decrease in chip size, chip density and frequency has made power consumption a major issue. Although the multi-core technology delivers a lot but it faces a number of thermal and power issues. High peak temperatures imbalanced the temperature gradients and affect the reliability of the system and increasing the cooling cost. So the main purpose of this research is power optimization and we specifically focus on those techniques which minimize energy consumption with very small impact on performance. This will not only include optimization policies for embedded systems but also include system-level, thread level power management techniques for multiprocessors, multi-core processor and real time embedded systems [2]

Three techniques of power optimization are used in Global schedulers 1) Dynamic Voltage and Frequency Scaling (DVFS) 2) Dynamic Power Management (DPM) 3) Dynamic Thermal management (DTM). DVFS adjusts the voltage and frequency in such a way that minimum energy is consumed. DVFS algorithms find the best setting that saves the maximum power while sacrificing the minimum speed. DPM is a design technology which reconfigures the whole electronic system dynamically in such a way that requested services can be provided with the minimum number of active components with suitable performance levels [3][4],[5]. DPM technique, selectively turn off all those components which are not in use. DPM is used in several portable systems but its applications are not yet explored because of the complexity of interfacing heterogeneous components. The

fundamental problem in implementation of DPM techniques is non-uniform workload during execution time [6]. To solve this problem DPM use predictive algorithm which predicts the future workload by using different predictive models. It covers several system level DPM approaches to save energy DTM technique is used to find an optimal solution to avoid peak temperature which causes hot spots on chips. Energy is not directly affected by temperature, but when temperature increases from threshold value some cooling mechanism is required to reduce the temperature. Cooling mechanism consume electricity to reduce the temperature so if some temperature management techniques are introduced it decreases the cooling cost [14], [15].

II. Background

A. Power Dissipation Basics

Most of the electronics circuits aim to give maximum performance while using minimum power. Electronics circuits are viewed as combination of different Complementary Metal Oxide Semiconductor (CMOS) devices. CMOS devices are the basic building block of all computing systems. CMOS semiconductor use negative polarity metal oxide semiconductor (NMOS) or positive polarity metal oxide semiconductor (PMOS). CMOS circuits consume less power as compared to other devices which are using just one type of transistor. This property makes them unique for usage in embedded systems which are mostly battery operated [13].

Power consumed in the CMOS is divided into three major components. These components are 1) dynamic power 2) static power 3) short circuit power. Among these three components dynamic power is the most dominant component.

$$P_{Total} = P_{Dynamic} + P_{Static} \quad (1)$$

Dynamic power is also known as switching power. Dynamic power can be calculated by using the given formula

$$P_{Dynamic} = C.K.V_{dd}^2.f \quad (1.1)$$

Where C is the load capacitance, K is the average number of switches or transitions per clock cycle V_{dd} is the supply voltage which is equal to the switching voltage in most of the cases and f is the clock frequency. In a single core processor if we increase the frequency by 50% roughly increase the power consumption two times, however in dual-core systems power consumption increases 30%. If we increase the supply voltage by keeping frequency constant power increases more rapidly because power is directly proportional to the square of supply voltage. To optimize the dynamic power we can reduce the working frequency which saves considerable amount of power but causes the performance degradation. In the same way reducing the supply voltage, reduces the dynamic power almost four times but it has an overhead by decreasing supply voltage circuit delay is increased so the circuit cannot be operate at the same working frequency. If we decrease supply voltage and frequency dynamic power decreases cubically but increases the execution time linearly [17], [18].

Second major component of power dissipation is static power which is due to leakage current [3]. This power consumption occurs when circuit is not changing states. Leakage current along with power supply causes static power consumption. The sources of leakage power are sub threshold leakage, p-n junction leakage and gate leakage. But the dominant factor is sub threshold leakage which represents the power dissipated by the transistor when it is deliberately to be off. Leakage power consists of almost 20 to 40 percent of total power dissipation [16].

Leakage power is also dependent on temperature as the temperature raises leakage power increases exponentially. Multiple efforts have been taken to reduce static power dissipation at processor and micro architectural level [7], [8].

Third component of power dissipation is short circuit power which is very low as compared to dynamic and static power. Short circuit power is the power dissipated when both PMOS and NMOS are on for a short period of time. Its means when both PMOS and NMOS are on then there is a direct path between supply voltage and ground. Due to small impact of short circuit power on total power has not drawn much attention of researchers.

B. Effects of Temperature on Power Consumption

As the chip *size* is shrinking and numbers of transistors are increasing per unit area on chip this leads more power consumption, more chip complexity and increases the temperature of the chip. Peak temperature reduces the lifespan of the chip, affects its performance and also increases the cooling cost [9]. To reduce peak temperatures additional cooling efforts are required, a typical cooling fan can consume 51% power budget of the server [10], [11].

Leakage power is strongly dependent on temperature. Leakage current increases the temperature which increases the leakage power consumption. Leakage power is increasing as the technology grows up according to ITRS roadmap [12] a graph is shown with the passage of time. In section 5 we will see how these problems are solved by using Dynamic thermal management policies.

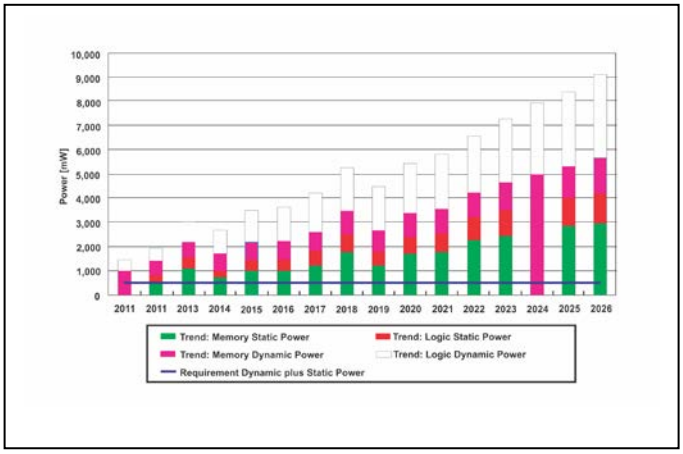

Fig 1 System on Chip Portable Power Consumption Trend [19]

III. Proposed Technique

A. *Pseudo Code*

```
Counter 1=Count_times
Config_k=number_core config
Config_R=number_core config_running
Config_N=next_core config_select
t1=max_temp_allowed of cores
t2=max_temp_running core
tmax=maximum_temp_configuration
minimum_counter=minimum value of counter
for (1 to total number of configuration)
If(number_coreconfig_running==number_core
config_Select)
Count_times++;
Else
No change in Values of counter
At each time Interval of Scheduler
If (Max_temp_Configuration < Max_temp_allowed)
{
No change}
elseif (Max_temp_configuration==Max_temp_allowed)
{
Continue with same
next_Core config_select <-Number_core config_select;
Change status from sleep mode to idle mode
}
Elseif(Maximum_temp_Configuration==Max_temp_runnin
g core)
Switch workload to next _core config-select;
{
number_core config_running=Next_core config_select
}
end if
```

IV. . Experimental Technique

Total power = dynamic power + static power……. (I)

Dynamic power = C × F × V ……..…….. (II)
Therefore C is the switching capacitance.
F is the frequency and V is the supply voltage
Static power = Leakage current × V…… (III)

Table I: The constraints of the chip

Parameters	Units	Meanings
z_1	M	Layer 1 Thickness
$d=z_2-z_1$	M	Layer 2 Thickness
K_1	W/mK	Layer 1 thermal conductivity
K_2	W/Mk	Layer 2 thermal conductivity
a_1	m^2/s	Layer 1 thermal diffusivity
a_2	m^2/s	Layer 2 thermal diffusivity
h_1	w/m^2k	Conductance b/w layer 1 & 2
h_2	w/m^2k	Conductance b/w layer 2 & ambient
L	M	Width

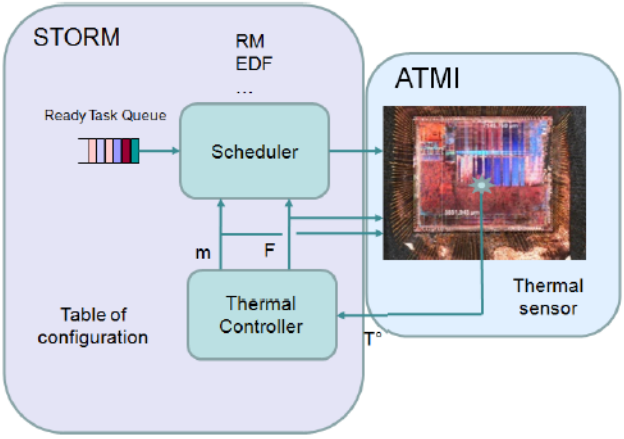

Figure 1: Block Diagram of Temperature controller Model

Table II: Configurations of cores

Frequency MHz	Utilization Factor %	No of cores in running state	No of cores in sleep mode
100	0-7	1	3
100	7-15	2	2
100	16-22	3	1
100	22-27	4	0

V. Experimental Results

In this section we discuss our experimental results that illustrates the temperature variation between the curves of proposed EDF and Global EDF'. Proposed EDF considers reliability and performance parameter so only those cores are in running state that is in working condition. In the beginning exponentially temperature on chip rises and then arrive at a steady state level. At 17% utilization factor the global EDF has 4.3℃ more temperature on chip as compare to our proposed approach. Proposed EDF based on core configurations and using quad-core processor.

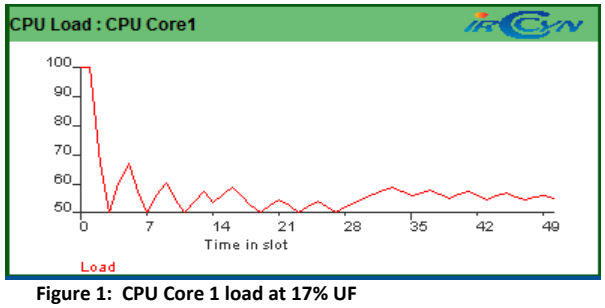

Figure 1: CPU Core 1 load at 17% UF

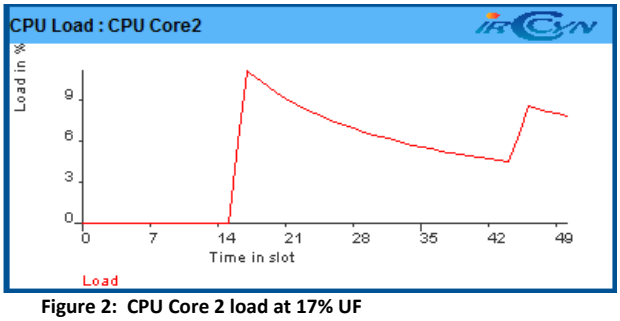

Figure 2: CPU Core 2 load at 17% UF

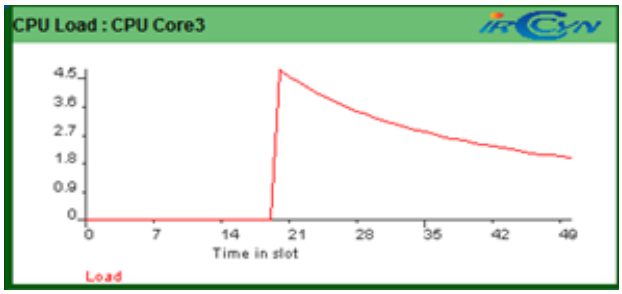

Figure 3: CPU Core 3 load at 17% UF

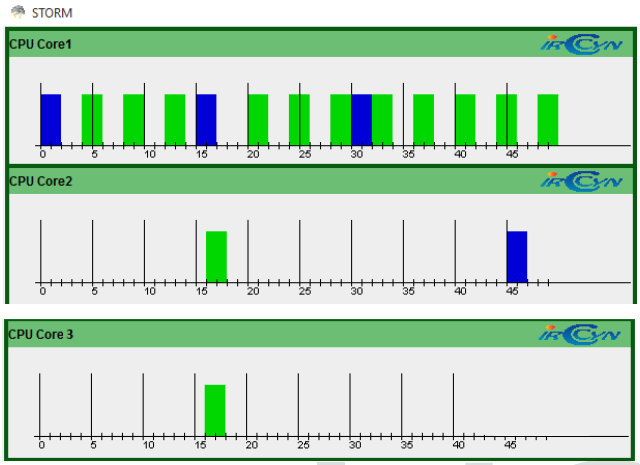

Figure 4: Gantt diagram for 3-running CPU's at 17% Uf

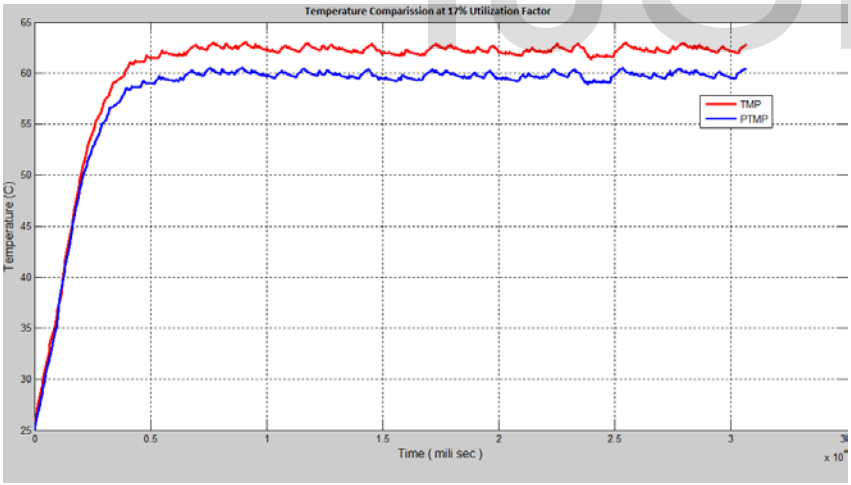

Figure 5: Temperature's variation at 17% UF on 25℃ ambient temperature

VI. CONCLUSION AND FUTURE WORK

With ever increasing processor speed and power densities in high speed performance systems, energy optimization and power management techniques have become an active research area. The paper summarizes the important research work done in the area. It discusses the principle and significance of Dynamic Voltage and Frequency Scaling (DVFS), Dynamic Power Management (DPM) and Dynamic Thermal Management (DTM) techniques and their extensions. Furthermore it highlights the trade-offs involved in designing and implementation of different techniques along with several practical applications and new challenges.

Most of the current techniques do not consider the impacts of ambient temperature which can be investigated in future work. Furthermore, most of the existing algorithms address homogeneous multi-core systems that can be extended to heterogeneous platforms. Another area which is not well explained is thermal management of 3-D integrated circuits. Most of the current techniques are based on 2-D integrated circuits. For this new plan novel thermal management techniques needs to be investigated.

REFERENCES

[1] Gorden E. Moore "Predicts the Future of Integrated Circuits". Computer History Museum. Electronics Magzine, April 1965.

[2] A. Biondi and G. Buttazzo, "Modeling and Analysis of Engine Control Tasks Under Dynamic Priority Scheduling", IEEE Transactions on Industrial Informatics, vol. 14, no. 10, pp. 4407-4416, 2018.

[3] S. Asyaban and M. Kargahi, "Feasibility Interval for Fixed-Priority Scheduling of Mixed-Criticality Periodic Tasks with Offsets", IEEE Embedded Systems Letters, pp. 1-1, 2018

[4] D. Konar, K. Sharma, V. Sarogi and S. Bhattacharyya, "A Multi-Objective Quantum-Inspired Genetic Algorithm (Mo-QIGA) for Real-Time Tasks Scheduling in Multiprocessor Environment", Procedia Computer Science, vol. 131, pp. 591-599, 2018.

[5] T. J. Semiconductor, B. Doyle, M. Group, and I. Corporation, "Transistor Elements for 30 nm Physical Gate Length And Beyond," Int'l Technology J., vol. 6, pp. 42-54, 2002.

[6] S. Yang, M. Powell, B. Falsafi, K .Roy, and T. Vijay kumar, "An Integrated Circuit/Architecture Approach to Reducing Leakage in Deep-Submicron High-Performance I-caches,"Proc. S-eventh Int'l Symp. High-Performance Computer Architecture(HPCA '01), pp. 147-157, 2001.

[7] S. Kaxiras, Z. Hu, and M. Martonosi, "Cache Decay: Exploiting Generational Behavior to Reduce Cache Leakage Power," Proc. Int'l Symp. Computer Architecture (ISCA '01), pp. 240-251, 2001.

[8] K. Skadron, M. Stan, K. Sankaranarayanan, W. Huang, S.Velusamy and D.Tarjan, "Temperature-Aware Microarchitecture Modeling and Implementation," In ACM Transaction On Architecture and Code Optimization, Vol. 1, Issue 1, pages 94 – 125, 2004.

[10] C. Lefurgy, K. Rajamani, F. Rawson, W. Felter, M. Kistler And T. Keller, "Energy Management for Commercial Servers," In *IEEE Computer*, Vol. 36, Issue 12, pages 39 – 48,2003.

[11] R. Ayoub, S. Sharifi and T. Rosing, "GentleCool: Cooling Aware -+ pages 295 – 298, 2010.

[12] M. Bohr , R. Chau, T. Ghani , and K. Mistry , " The High-k Solution, " IEEE Spectrum, vol. 44, no. 10, pp. 29-35 , Oct. 2007.

[13] T.J. Semi-conductor , B. Doyle, M. Group, and I. Corporation, " Transistor Elements for 30 nm Physical Gate Lengths and Beyond," Int'l Technology J., vol. 6, pp. 42 -54, 2002.

[14] S. Yang, M. Powell, B. Falsafi, K. Roy, and T. Vijay kumar, " An Integrated Circuit / Architecture Approach to Reducing Leakage in Submicron High-Performance I-caches, " Proc. Seventh Int'l Symp. High- Performance Computer Architecture (HPCA '01), pp. 147-157, 2001.

[15] Li-Chuan , Xiao Jun , Bin Liu, " A Survey on Power Optimization Techniques, " IEEE International Workshop on System-on-Chip, 2003.

[16] S. Kaxiras, Z. Hu, and M. Martonosi, "Cache Decay : Exploiting Generational Behavior to Reduce Cache Leakage Power ," Proc.Int'l Symp. Computer Architecture (ISCA '01), pp. 240-251, 2001.

[17] C.-h. Hsu and W.-c. Feng, " A power-aware run-time system for high-performance computing ," in Proceedings of the 2005 ACM/IEEE conference e on Supercomputing. IEEE Computer Society,2005.

[18] R. Xu, D. Zhu, C. Rusu, R. Melhem , and D. Moss´e, "Energy-efficient policies for embedded clusters," In ACM SIGPLAN Notices, vol. 40, no. 7, pp. 1–10, 2005.

[19] T. Horvath, T. Abdelzaher, K. Skadron, and X. Liu, "Dynamic voltage scaling in multitier web servers